In The Claims:

Please amend the Claims as follows:

1-2. (Canceled)

3. (Currently Amended) An integrated circuit connected to a transmission line, the integrated circuit comprising:

a driver including a plurality of driving units for outputting data to the transmission line and receiving data from the transmission line; and

a controller for applying a plurality of control signals to the driver, the control signals being generated in response to an output activation signal and at least one impedance code signals related to states of the impedance of the transmission line,

wherein at least one driving unit is driven in response to the control signals, and the driver includes an on-chip termination circuit for impedance matching external devices,

wherein the driver includes a first driving unit and a second driving unit commonly connected to the transmission line,

~~The integrated circuit of claim 2,~~ wherein the controller includes:

a circuit for generating a first up driving control signal in response to the output activation signal and the output data signal;

a circuit for generating a second up driving control signal in response to the output activation signal and the output data signal;

a circuit for generating a first down driving control signal in response to the output activation signal and the output data signal;

a circuit for generating a second down driving control signal in response to the output activation signal and the output data signal;

a circuit for generating a third up driving control signal in response to the output activation signal, the output data signal and a first impedance code signal;

a circuit for generating a fourth up driving control signal in response to the output activation signal, the output data signal, the first impedance code signal and a second impedance code signal;

a circuit for generating a third down driving control signal in response to the output activation signal, the output data signal and the first impedance code signal; and

a circuit for generating a fourth down driving control signal in response to the output activation signal, the output data signal, the first impedance code signal and the second impedance code signal.

4. (Original) The integrated circuit of claim 3, wherein the first driving unit includes:

a first up driver for connecting a power supply voltage with the transmission line in response to the first up driving control signal;

a second up driver for connecting the power supply voltage with the transmission line in response to the second up driving control signal;

a first down driver for connecting the transmission line with a ground voltage in

response to the first down driving control signal; and

a second down driver for connecting the transmission line with the ground voltage in response to the first down driving control signal.

5. (Original) The integrated circuit of claim 4, wherein the first up driver includes at least one PMOS transistor, the PMOS transistor connecting the power supply voltage with the transmission line in response to the first up driving control signal.

6. (Original) The integrated circuit of claim 4, wherein the second up driver includes at least one PMOS transistor, the PMOS transistor connecting the power supply voltage with the transmission line in response to the second up driving control signal.

7. (Original) The integrated circuit of claim 4, wherein the first down driver includes at least one NMOS transistor, the NMOS transistor connecting the transmission line with the ground voltage in response to the first down driving control signal.

8. (Original) The integrated circuit of claim 4, wherein the second down driver includes at least one NMOS transistor, the NMOS transistor connecting the transmission line with the ground voltage in response to the second down driving control signal.

9. (Original) The integrated circuit of claim 4, wherein the second up driver and the second down driver are contained in the on-chip termination circuit.

10. (Original) The integrated circuit of claim 9, wherein the first up driver and the first down driver are selectively driven according to states of the output data signals at a data output operation, and the second up driver and the second down driver are simultaneously driven at a data input operation.

11. (Original) The integrated circuit of claim 4, wherein the second driving unit includes:

a third up driver for connecting the power supply voltage with the transmission line in response to the third up driving control signal;

a fourth up driver for connecting the power supply voltage with the transmission line in response to the fourth up driving control signal;

a third down driver for connecting the transmission line and the ground voltage in response to the third down driving control signal; and

a fourth down driver for connecting the transmission line with the ground voltage in response to the fourth down driving control signal.

12. (Original) The integrated circuit of claim 11, wherein the third up driver includes at least one PMOS transistor, the PMOS transistor connecting the power

supply voltage with the transmission line in response to the third up driving control signal.

13. (Original) The integrated circuit of claim 11, wherein the fourth up driver includes at least one PMOS transistor, the PMOS transistor connecting the power supply voltage with the transmission line in response to the fourth up driving control signal.

14. (Original) The integrated circuit of claim 11, wherein the third down driver includes at least one NMOS transistor, the NMOS transistor connecting the transmission line with the ground voltage in response to the third down driving control signal.

15. (Original) The integrated circuit of claim 11, wherein the fourth down driver includes at least one NMOS transistor, the NMOS transistor connecting the transmission line with the ground voltage in response to the fourth down driving control signal.

16. (Original) The integrated circuit of claim 11, wherein the fourth up driver and the fourth down driver are contained in the on-chip termination circuit.

17. (Original) The integrated circuit of claim 16, wherein the third up driver and

the third down driver are selectively driven simultaneously together with the first up driver and the first down driver according to kinds of the output data signals at the data output operation, and the fourth up driver and the fourth down driver are driven simultaneously together with the second up driver and the second down driver at the data input operation.

18. (Canceled)

19. (Currently Amended) An integrated circuit for inputting/outputting data through a transmission line, the integrated circuit comprising:

a circuit for generating a first up driving control signal from an output data signal in response to an output activation signal;

a circuit for generating a first down driving control signal from the output data signal in response to the output activation signal;

a circuit for generating a second up driving control signal from the output data signal in response to the output activation signal;

a circuit for generating a second down driving control signal from the output data signal in response to the output activation signal;

first PMOS transistor circuit for connecting a power supply voltage with the transmission line in response to the first up driving control signal;

first NMOS transistor circuit for connecting the transmission line with a ground voltage in response to the first down driving control signal;

second PMOS transistor circuit for connecting the power supply voltage with the transmission line in response to the second up driving control signal; and

second NMOS transistor circuit for connecting the transmission line with the ground voltage in response to the second down driving control signal,

wherein the first and second PMOS transistor circuits and the first and second NMOS transistor circuits are selectively driven in response to the first and second up driving control signals and the first and second down driving control signals according to states of the output data signals at the data output operation, and the second PMOS transistor circuit and the second NMOS transistor circuit are simultaneously driven at the data input operation; ~~The integrated circuit of claim 18, further comprising:~~

a circuit for inputting the output data signal and generating a third up driving control signal in response to the output activation signal and a first code signal related to the impedance;

a circuit for inputting the output data signal and generating a third down driving control signal in response to the output activation signal and the first code signal related to the impedance;

a circuit for inputting the output data signal and generating a fourth up driving control signal in response to the output activation signal, the first code signal and a second code signal related to the impedance;

a circuit for inputting the output data signal and generating a fourth down driving control signal in response to the output activation signal and the first and second code signals;

third PMOS transistor circuit for connecting the power supply voltage with the transmission line in response to the third up driving control signal;

third NMOS transistor circuit for connecting the transmission line with the ground voltage in response to the third down driving control signal;

fourth PMOS transistor circuit for connecting the power supply voltage with the transmission line in response to the fourth up driving control signal; and

fourth NMOS transistor circuit for connecting the transmission line with the ground voltage in response to the fourth down driving control signal,

wherein the PMOS transistor circuits and the NMOS transistor circuits are selectively driven according to states of the output data signals at the data output operation, and the second and fourth PMOS transistor circuits and the second and fourth NMOS transistor circuits are simultaneously driven at the data input operation.

20. (Canceled)

21. (New) A method for matching impedance for an integrated circuit connected to a transmission line, comprising:

generating a first up driving control signal from an output data signal in response to an output activation signal;

generating a first down driving control signal from the output data signal in response to the output activation signal;

generating a second up driving control signal from the output data signal in

response to the output activation signal;

generating a second down driving control signal from the output data signal in response to the output activation signal;

connecting a power supply voltage with the transmission line in response to the first up driving control signal;

connecting the transmission line with a ground voltage in response to the first down driving control signal;

connecting the power supply voltage with the transmission line in response to the second up driving control signal; and

connecting the transmission line with the ground voltage in response to the second down driving control signal,

wherein the first and second PMOS transistor circuits and the first and second NMOS transistor circuits are selectively driven in response to the first and second up driving control signals and the first and second down driving control signals according to states of the output data signals at the data output operation, and the second PMOS transistor circuit and the second NMOS transistor circuit are simultaneously driven at the data input operation;

inputting the output data signal and generating a third up driving control signal in response to the output activation signal and a first code signal related to the impedance;

inputting the output data signal and generating a third down driving control signal in response to the output activation signal and the first code signal related to the impedance;

inputting the output data signal and generating a fourth up driving control signal in response to the output activation signal, the first code signal and a second code signal related to the impedance;

inputting the output data signal and generating a fourth down driving control signal in response to the output activation signal and the first and second code signals;

connecting the power supply voltage with the transmission line in response to the third up driving control signal;

connecting the transmission line with the ground voltage in response to the third down driving control signal;

connecting the power supply voltage with the transmission line in response to the fourth up driving control signal; and

connecting the transmission line with the ground voltage in response to the fourth down driving control signal,

wherein the PMOS transistor circuits and the NMOS transistor circuits are selectively driven according to states of the output data signals at the data output operation, and the second and fourth PMOS transistor circuits and the second and fourth NMOS transistor circuits are simultaneously driven at the data input operation.